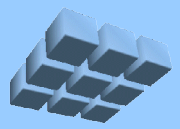
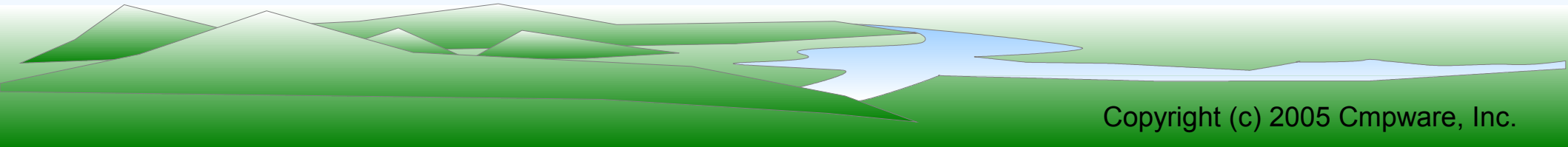


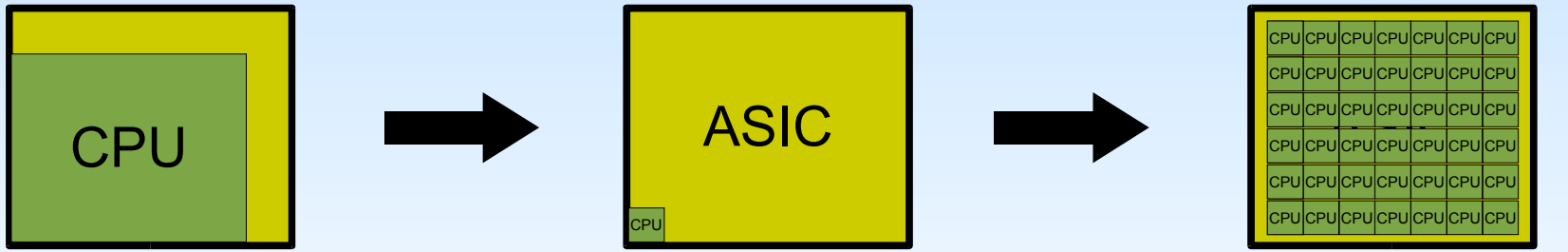
# Modeling Multiprocessors in the Cmpware CMP-DK

Cmpware, Inc.

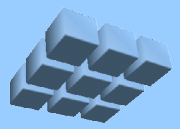


# Introduction

- One billion transistors available (2005)
- 1B transistor custom designs very expensive
- Emerging trend: *multiprocessors*
  - Large, programmable IP blocks (CPUs)
  - Thousands of CPUs / millions of MIPS




2000 SoC 2005 SoC 2005 MP-SoC



# Cmpware CMP-DK

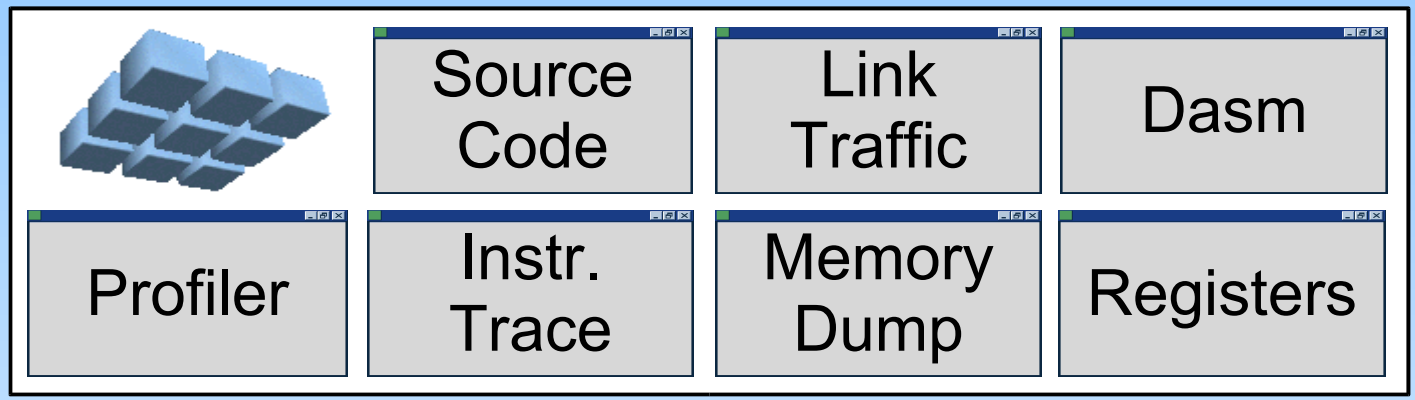
- Cmpware Configurable Multiprocessor Development Kit (CMP-DK)
- *"Build fast multiprocessor models, fast"*
- Plugs in to *Eclipse*-based IDE
- Models (dynamically) built from:
  - **Processors**: Store and process data
  - **Networks**: A collection of links
  - **Links**: Transfer data between processors
- Simulates at the *processor* level

CPU Model

Network Model

Link Model

# The Cmpware Toolkit




CPU Compiler / Tools

ELF / DWARF Loader

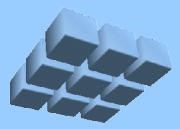

***Cmpware*** Multiprocessor Simulation Engine

CPU Model

Network Model

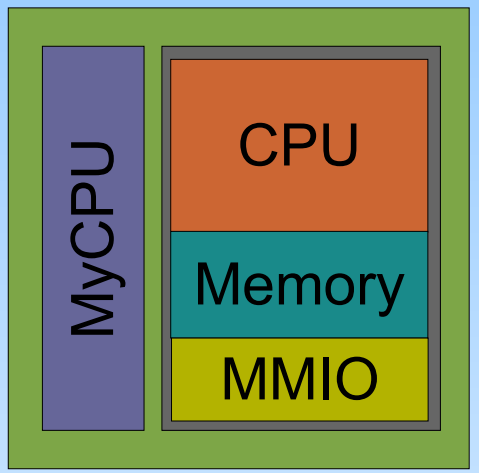
Link Model

"pluggable" models



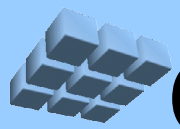
# The Processor Models

CPU Model



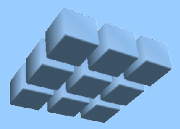

- Processor (CPU):
  - Common interface to simulator
  - Simulation machinery
  - Run-time statistics gathering
- Memory:  standard memory array
- MMIO:  Memory Mapped IO

==> *Standard processor model customized with processor description modules*



# Customizing the Processor Model

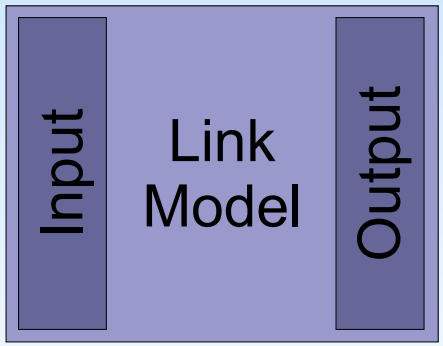
- Define methods for:
  - **`decode()`** - The instruction decode
  - **`execute()`** - The instruction execution
  - **`getPC()/setPC()`** - Access Program Counter
  - **`dasm()`** - Disassembly
- *ProcGen* tool helps build these methods
- Models run at 1M – 2M cycle per second
- Models have built-in profiling, cycle counting, power estimation, instruction count, others.

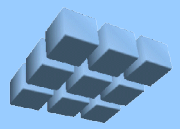


# The Link Model

Link Model

- A generic data communication path
- Implements **`read()`** / **`write()`** and status / control / synchronization methods
- Used to connect processors
- Has *input* and *output* interfaces
- Examples:
  - FIFO
  - Bus
  - Shared Register



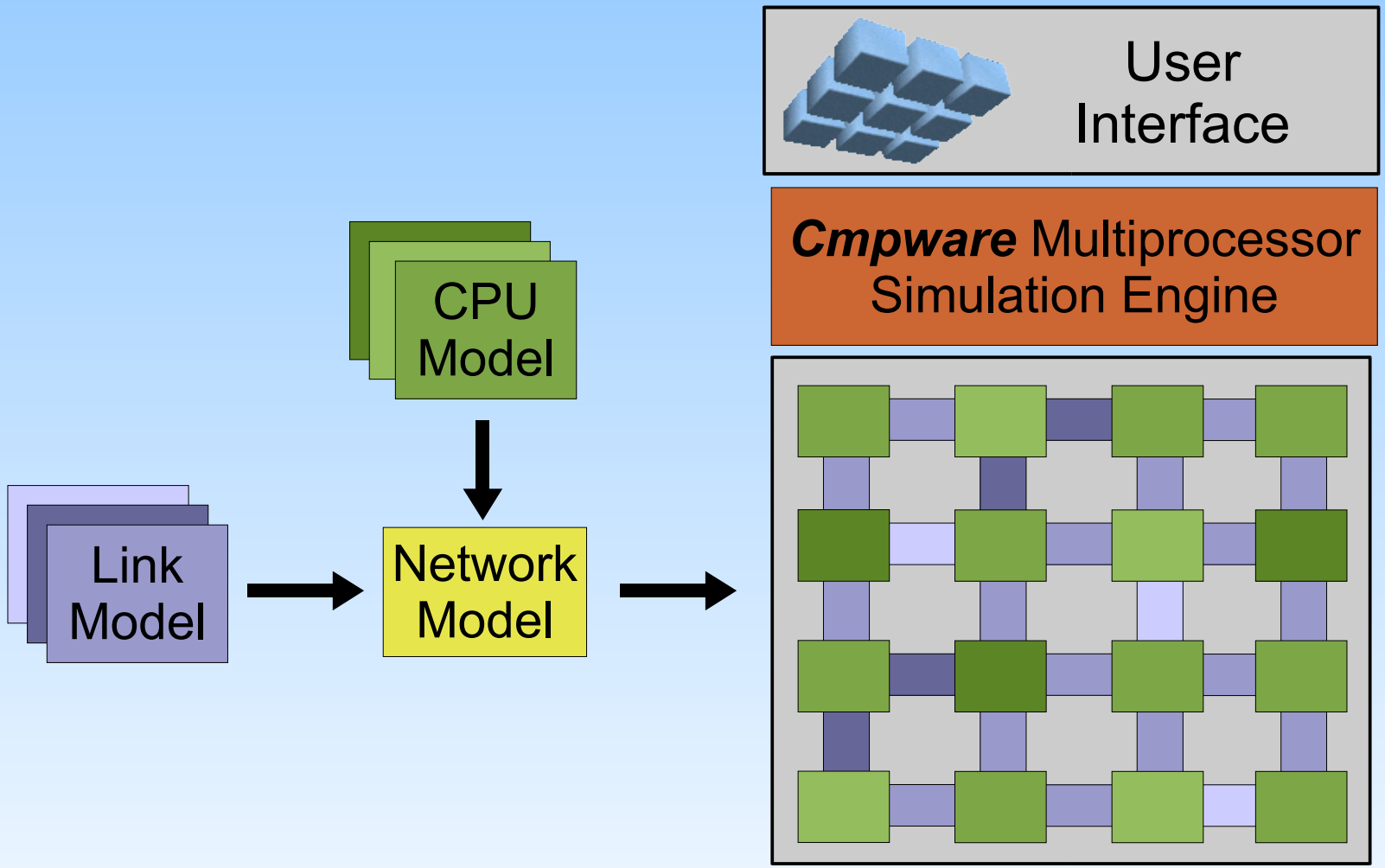


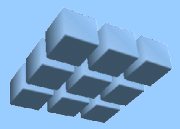
# The Network Model

Network Model

- Connects collection of *Links* to processors
- Often parameterized for the processor array
- Not an actual simulation object; a recipe for connecting links to processors
- Examples:
  - Mesh
  - Torus
  - Hypercube
  - Custom interconnect

# The Multiprocessor Model

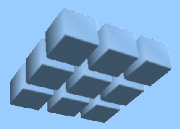




# The Multiprocessor Simulation Engine

- Coordinates  simulation of processors
- Synchronizes processors
- Synchronizes communication
- Keeps system-level statistics
- Supplies data to user interface(s)
- The *'Control Center'*

***Cmpware*** Multiprocessor Simulation Engine



# The Cmpware Multiprocessor Simulation Environment

- Processor / Link based models
- Build processor models in a few hours
- Redefine multiprocessor in seconds
- Speeds simulation (1M+ cycles / second)
- Eclipse IDE plug-in

**==> *“Build fast multiprocessor models, fast”***