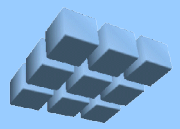
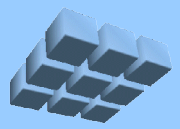


Reducing Power with Configurable Multiprocessing

Cmpware, Inc.

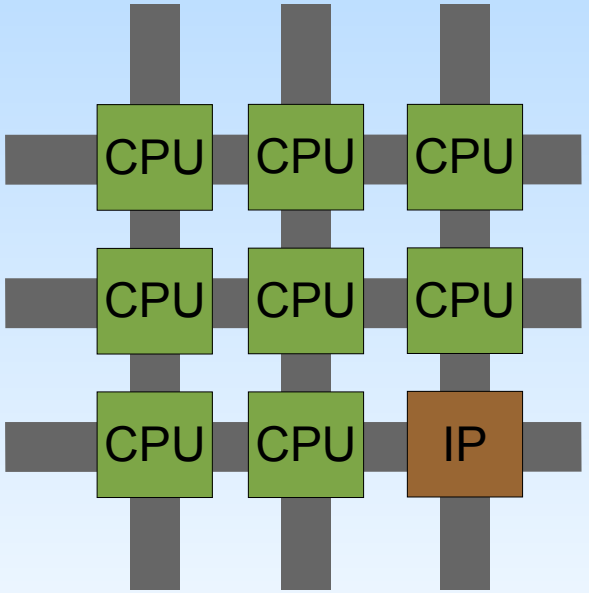


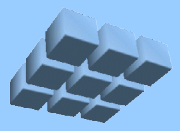
Introduction

- Power has become ***the*** limiting design factor
- Large designs now have 'power budgets'
- Large devices can generate 100W+, more than can effectively be dissipated
- Power increasingly important for handhelds
- Heat generation a problem for data and communication centers
- All other technology trends make power problems worse

Configurable Multiprocessing

- Thousands of CPUs on a die possible
- High performance: Millions of MIPS
- Simplifies HW design
- Simplifies HW verification
- Flexible
- Scalable
- Reprogrammable
- ***Reduces power***



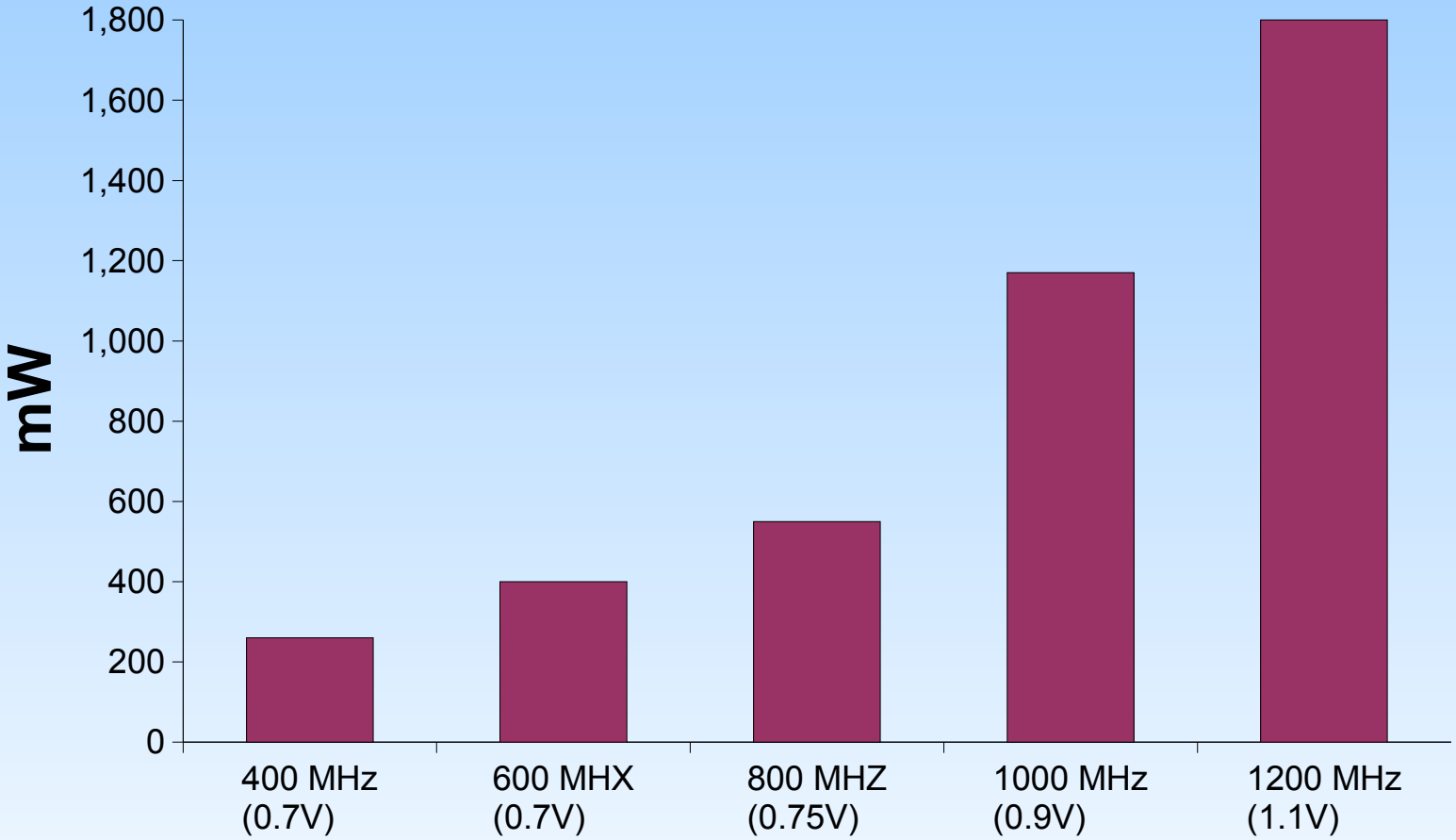


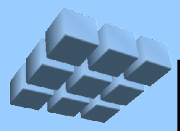
Voltage, Clock Speed and Power

- Faster clocks need higher voltages
- Power proportional to voltage squared (V^2)
- ARM1020E (Samsung “Halla”, 0.13 um)
  - 400 MHz / 0.7 V ==> 260 mW
  - 800 MHz / 0.75 V ==> 550 mW
  - 1200 Mhz / 1.1V ==> 1800 mW

==> *3x performance = approx. 7x power*

Voltage, Clock Speed and Power





More Processors == Lower Power

- Run hardware at lower voltage / clock speed
- Multiple processors meet performance goals

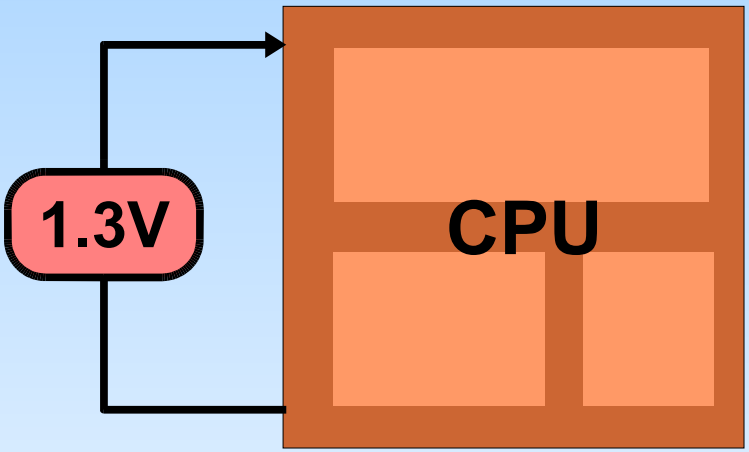
Processors	MIPS (total)	Power (total)
1 x ARM1020E	1 x 1200 = **1200**	1 x 1800 = **1800 mW**
3 x ARM1020Es	3 x 400 = **1200**	3 x 260 = **780 mW**

- One vs. Three ARM1020E ("Halla")
  - Identical raw performance (1200 MIPS)
  - **1800** vs. **780** mW: **57%** total power savings

    ==> *Add processors and save power (!)*

Configurable Multiprocessing

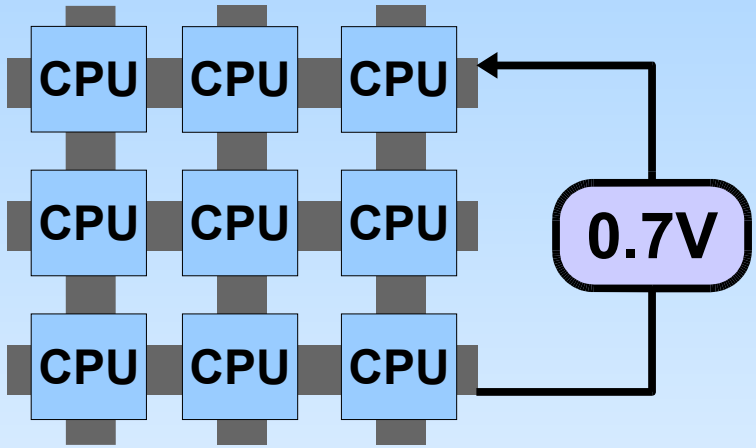
Desktop CPU



2 GHz

75 Watts

CMP Architecture

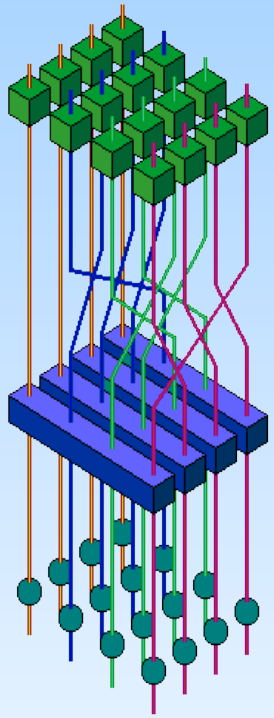


200 MHz

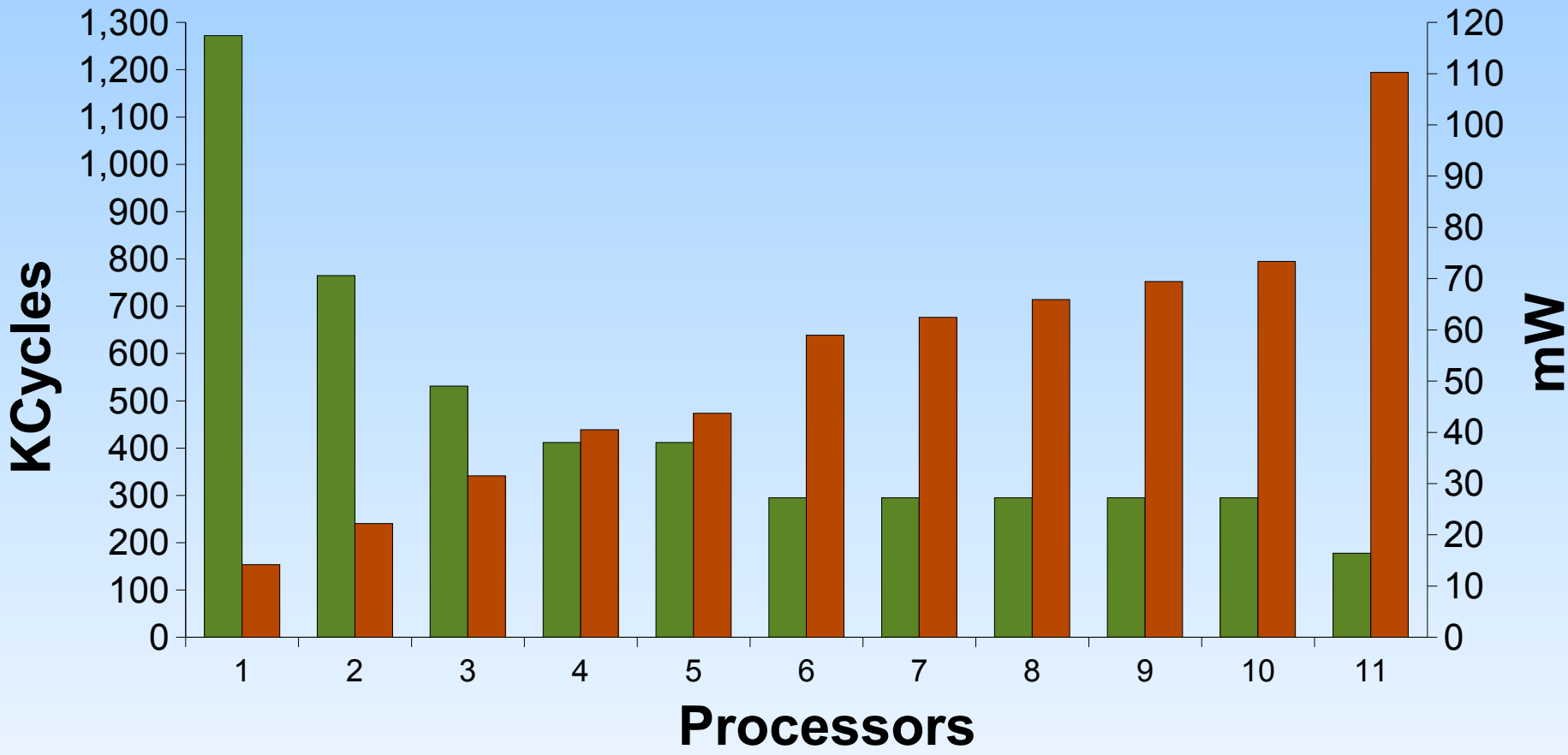
<2.5 Watts

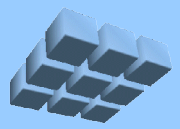
Example: AES Encryption

- AES: Advanced Encryption Standard
- US NIST program to replace the Data Encryption Standard (DES)
- Selected 'Rijndael' algorithm in 2000
- Efficient HW and SW implementations
- Runs on 1 to 11 nodes
- ***700%*** speedup with **11** processors



AES Performance / Power





Conclusions

- Use multiple processors to:
  - increase performance
  - Lower clock speed
  - Reduce power consumption
- Leverages quadratic dependence of power on voltage ($P \approx V^2$)
- Provides unique power / performance options