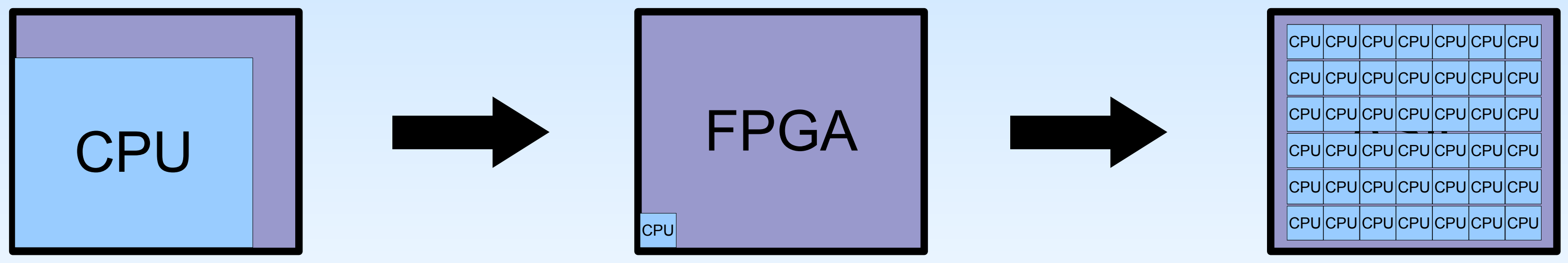
Software Development Tools for Soft Multiprocessors

Cmpware, Inc.

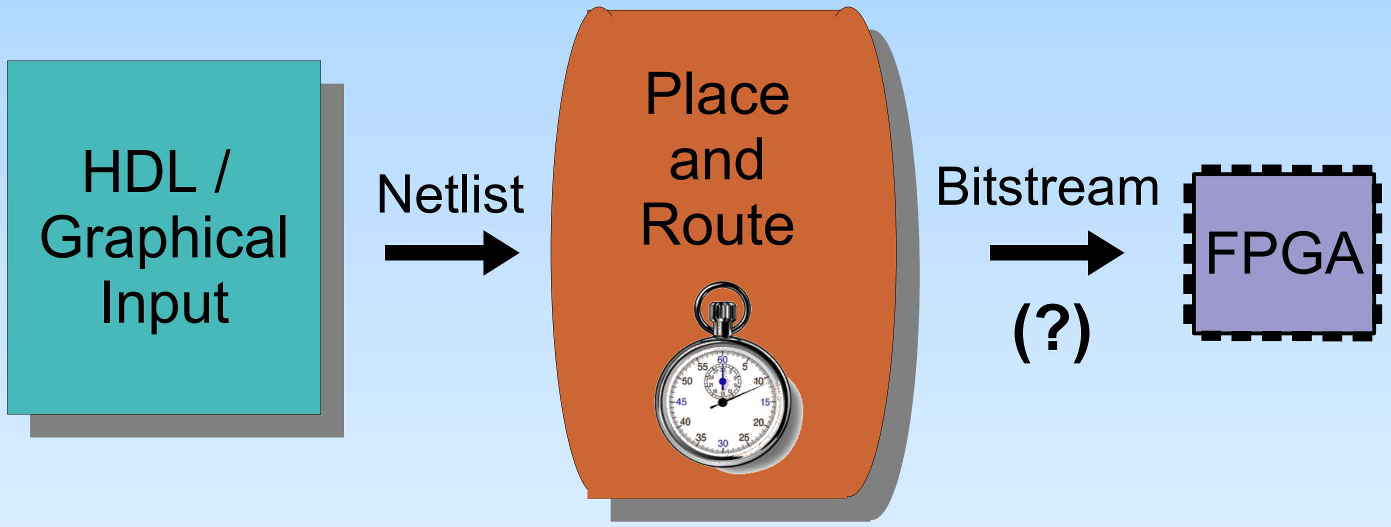
Soft Multiprocessors

- One billion transistor FPGAs available (2006)
- FPGA design becoming complex
- Emerging trend: *soft multiprocessors*
  - Large, programmable IP blocks (CPUs)
  - Hundreds of CPUs / thousands of MIPS



2002 Soft CPU — 2006 Soft CPU — 2006 Soft MP

The FPGA Tools Flow

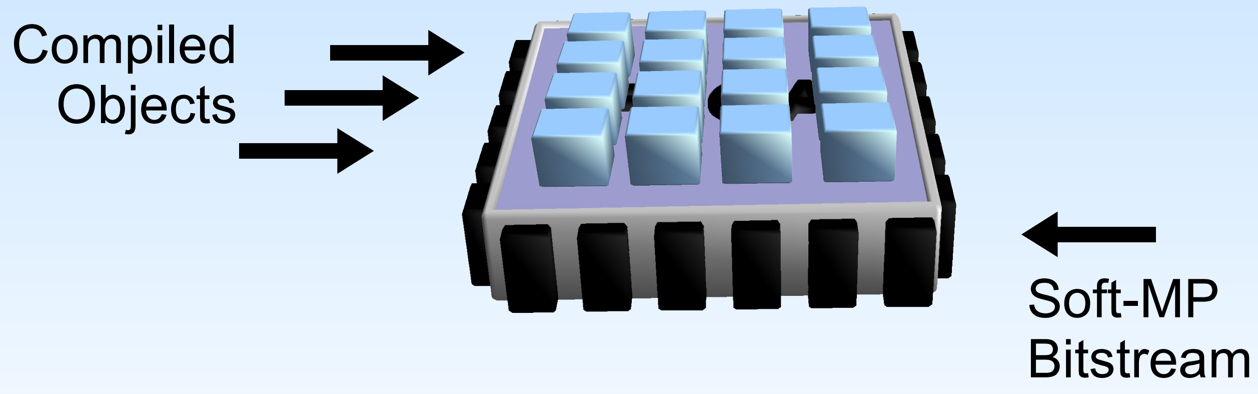


FPGA Tools Flow

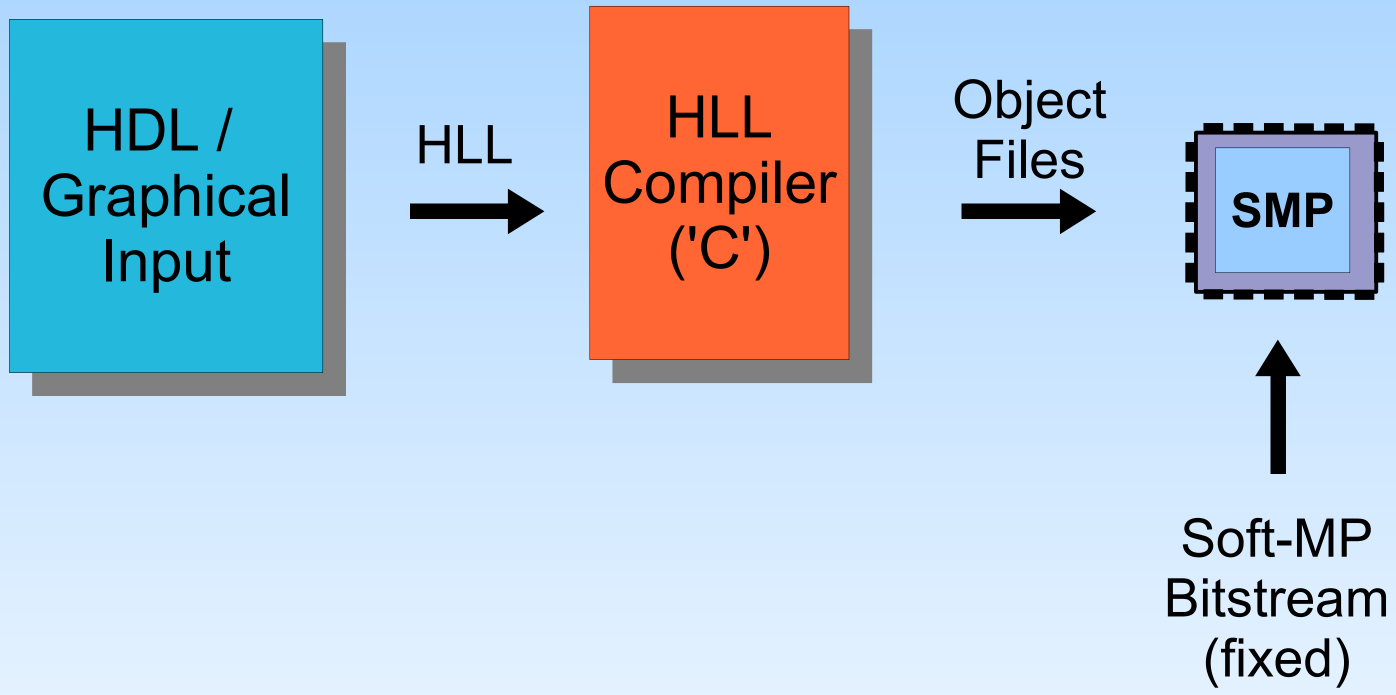
- Place and route slow (hours)
- Tools large and cumbersome
- Requires large, fast workstations
- Circuit size varies / difficult to estimate
- Circuit speed varies / difficult to estimate
- High / highly variable power consumption
- Hardware model inflexible

The Soft Multiprocessor Layer

- Use FPGA tools to define Soft-MP circuit
- Program Soft-MP / FPGA using standard programming languages (“C”)
- Multiprocessor software abstraction layer over FPGA hardware layer



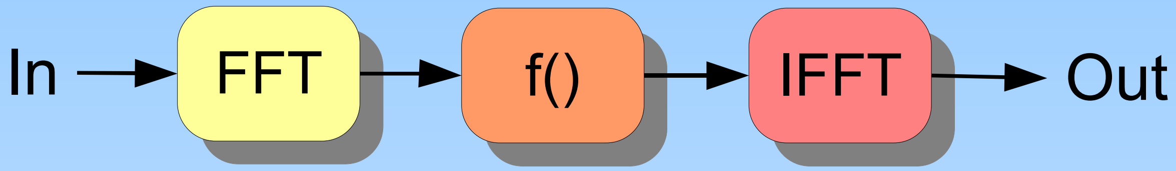
The Soft Multiprocessor Tool Flow



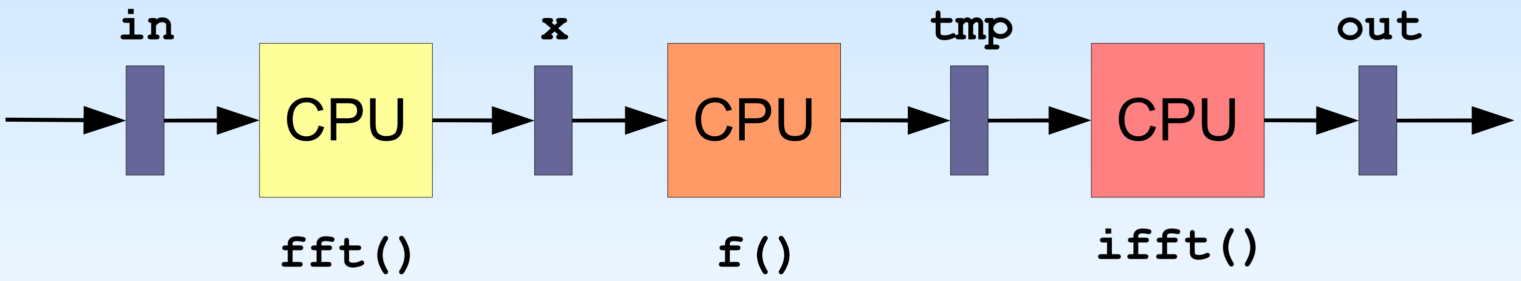
Soft Multiprocessor Tools Flow

- Standard HLL compilers
- Fast compilation (seconds)
- Smaller, simpler tool chain
- Circuit size and speed fixed
- Power consumption simple to estimate
- Very flexible model (software)
- Parallelization:
  - Graphical design has implicit partitioning
  - Blocks can be mapped directly to processors

Filtering Example: Task Level Parallelism



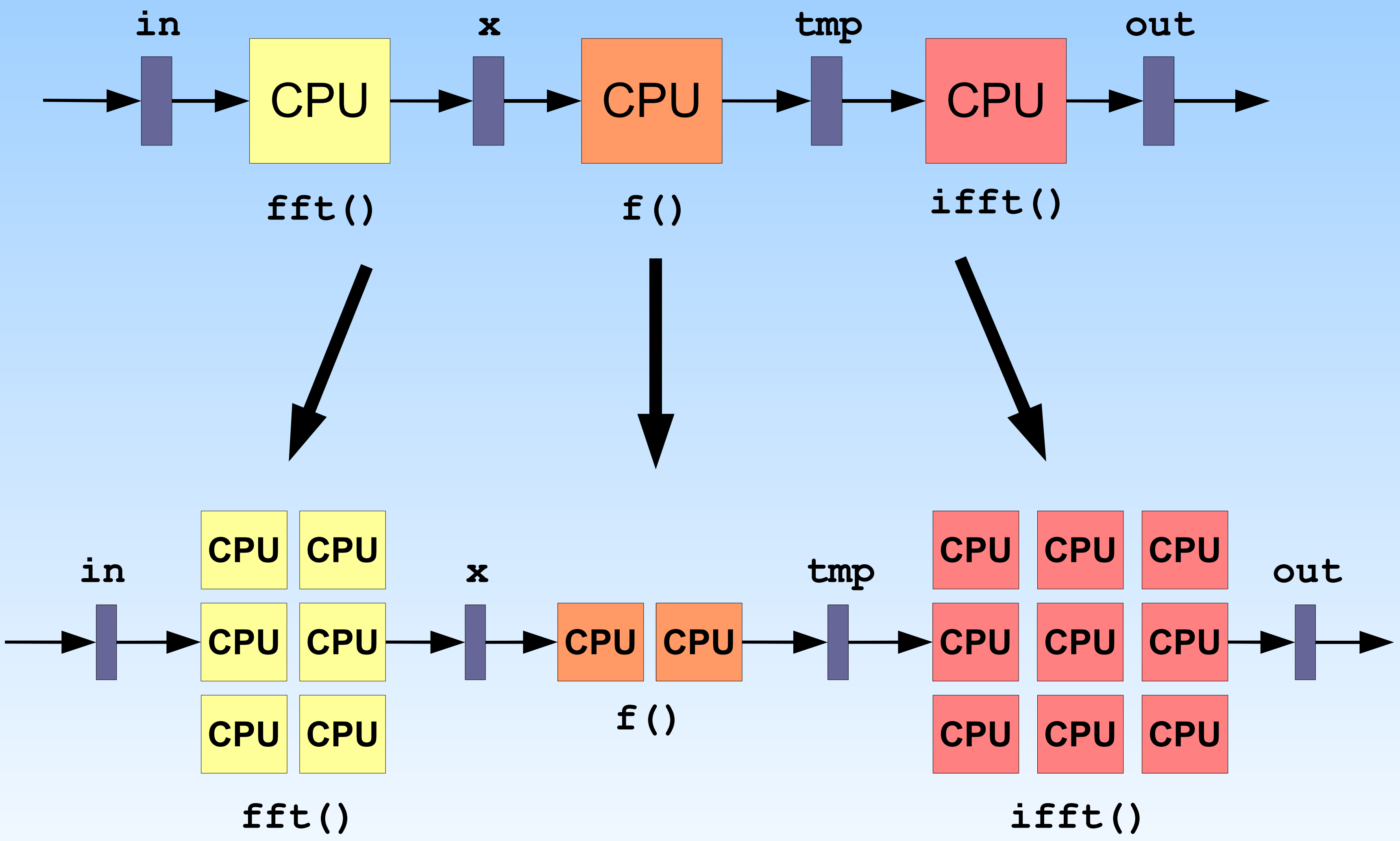
```
volatile int *x, *in, *tmp, *out;

*x = fft(*in);
*tmp = f(x);
*out = ifft(tmp);
```



Application Partitioning

- Graphical environments implicitly specify
  - Algorithm partitioning
  - Communication patterns
- Many graphical tools already generate “C”
- Place one or more 'nodes' per processor
- “Sub-task” partitioning also possible for higher performance

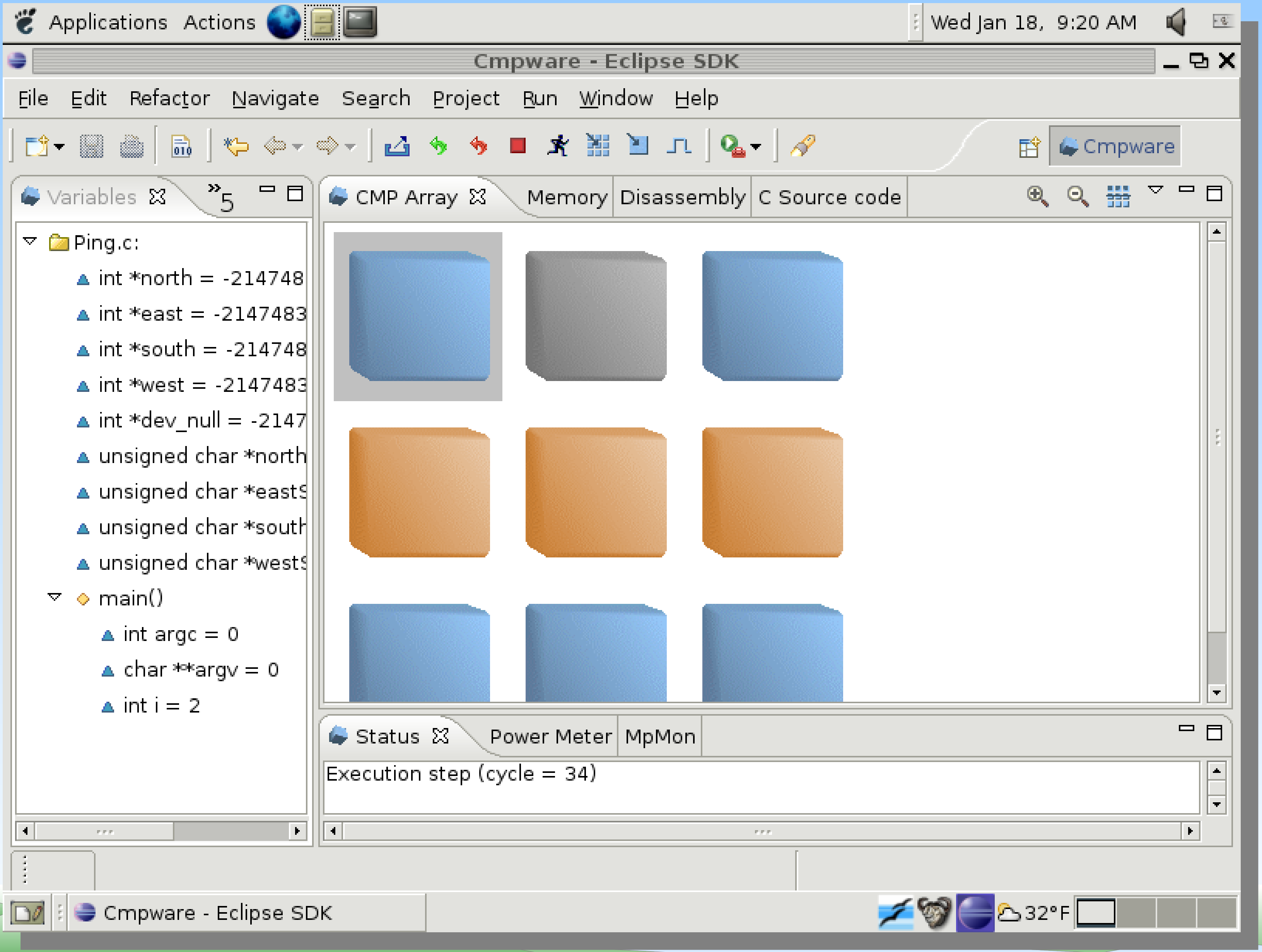
Filter Example: Sub-Task Level Parallelism



The Cmpware CMP-DK

- Useful for experimenting with soft multiprocessor / communications approaches
- Help to develop / debug tool chain
- Cmpware CMP-DK:
  - Quickly build and program multiprocessors
  - Redefine multiprocessor in seconds
  - Speeds simulation (2M+ instructions / second)
  - Complete Eclipse development environment
  - Standard models for NIOS, MicroBlaze, Sparc (LEON), MIPS32 and more

The Cmpware CMP-DK



```
Ping.c:
    int *north = -214748
    int *east = -2147483
    int *south = -214748
    int *west = -2147483
    int *dev_null = -2147
    unsigned char *north
    unsigned char *east9
    unsigned char *south
    unsigned char *west9
  main()
      int argc = 0
      char **argv = 0
      int i = 2
```

```
Execution step (cycle = 34)
```

Conclusions

- Soft multiprocessing:
  - Greatly improves (re-) programmability of FPGAs
  - Fast, simple graphical tools --> FPGA path
  - True software approach – no “HLL to HDL”
- Cmpware CMP-DK:
  - Experiment with Soft-MP
  - Explore processor / communication architectures
  - Powerful multiprocessor software development environment for test and debug